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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,843	11/29/2001	Harumitsu Miyashita	10407-010US (A1031MT-US1)	6402

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EXAMINER	
ORTIZ CRIADO, JORGE L	

ART UNIT	PAPER NUMBER
2655	3

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,843	MIYASHITA ET AL.	
	Examiner	Art Unit	
	Jorge L Ortiz-Criado	2655	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 4, 8 and 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiramatsu U.S. Patent No. 5,596,559.

Regarding claim 1, Hiramatsu discloses an apparatus for reproducing information that has been digitally recorded on a storage medium, the apparatus comprising:

a first waveform equalizer, which equalizes a read signal corresponding to the information read out from the storage medium, thereby outputting a first equalized signal (See Fig. 16, ref # 32; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31); and

a second waveform equalizer, which has an equalization characteristic different from that of the first waveform equalizer, outputs a second equalized signal and is selectively used to extract a read clock signal (See Fig. 16, ref #33; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Regarding claim 2, Hiramatsu discloses wherein the second equalized signal is used exclusively for extracting the read clock signal and the information is not extracted from the second equalized signal (See Fig. 16, ref #33; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Regarding clam 3, Hiramatsu discloses wherein the second waveform equalizer has such an equalization characteristic as to emphasize high-frequency components of an input signal more strongly than the first waveform equalizer does (See Fig. 16, ref #33; Fig. 12; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Regarding claim 4, Hiramatsu discloses clock generator for outputting the read clock signal responsive to the second equalized signal; and a decoder for generating digitized data from the first equalized signal (See Fig. 16, ref #37,36; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Regarding claim 6, Hiramatsu discloses wherein the decoder performs its decoding operation in accordance with a pattern of a digital read signal that has been obtained by sampling

the first equalized signal (See Fig. 16, ref #37,36; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Regarding claim 7, Hiramatsu discloses wherein the decoder operates in accordance with a PRML method (See Fig. 16, ref #36; col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Regarding claim 8, wherein the storage medium is an optical disk (See col. 5, line 56 to col. 6, line 52; col. 7, line 46 to col. 8, line31)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu U.S. Patent No. 5,596,559 in view of the "admitted prior art".

Regarding claim 5, Hiramatsu discloses all the limitations based on claim 4 as outlined above. Hiramatsu further discloses a phase shifter for shifting, responsive to a phase control signal, the phase of the read clock signal that has been output from the clock generator and

outputting a phase-shifted read clock signal as a sampling clock signal (See col. 7, line 61 to col. 8, line 2);

an A/D converter for converting the first equalized signal into a digital read signal by sampling the first equalized signal by reference to the sampling clock signal (See col. 8, lines 3-20; Fig. 16, ref #34; and

a phase control signal generator for detecting a phase deviation of the sampling clock signal in accordance with the digital read signal that has been output from an analog to digital converter (See col. 7, line 59 to col. 8, line 2; Fig. 16, ref# 35) and

outputting the phase control signal to the phase shifter so as to reduce the phase deviation of the sampling clock signal (See col. 7, line 59 to col. 8, line 2),

wherein the decoder generates the digitized data from the digital read signal that has been output from the A/D converter (See col. 7, line 59 to col. 8, line 20).

Hiramatsu discloses correcting the phase shift of the read clock signal to reducing the error rate and reproducing data accurately even from signal with high level variations, by applying the corrected read clock signal to the decoder that generates the digitized data from the digital read signal that has been output from the A/D converter by using the corrected read clock signal, hence correcting the first equalized signal outputted from the A/D converter.

But Hiramatsu does not expressly disclose wherein the A/D converter for converting the first equalized signal into a digital read signal by sampling the first equalized signal by reference to the sampling clock signal that has been output from the phase shifter and wherein the a phase control signal generator for detecting a phase deviation of the sampling clock signal in accordance with the digital read signal that has been output from the A/D converter.

However this feature is well known in the art as evidenced by the admitted prior art, which discloses a phase shifter for shifting, responsive to a phase control signal, the phase of the read clock signal that has been output from the clock generator and outputting a phase-shifted read clock signal as a sampling clock signal, an A/D converter for converting the equalized signal into a digital read signal by sampling equalized signal by reference to the sampling clock signal that has been output from the phase shifter; and a phase control signal generator for detecting a phase deviation of the sampling clock signal in accordance with the digital read signal that has been output from the A/D converter and outputting the phase control signal to the phase shifter so as to reduce the phase deviation of the sampling clock signal, wherein a decoder generates the digitized data from the digital read signal that has been output from the A/D converter (See page 2, paragraph [005] to page, 5 paragraph [0013]; Fig. 8).

Therefore, it would have been obvious to one with ordinary skill in the at the time of the invention to converting the first equalized signal into a digital read signal by sampling the first equalized signal by reference to the sampling clock signal that has been output from the phase shifter and wherein the a phase control signal generator for detecting a phase deviation of the sampling clock signal in accordance with the digital read signal that has been output from the A/D converter in order to appropriately control the phase of the read clock signal and reproduce data accurately by the decoder even from a signal with relatively high level of jitter fro intersymbol interference and further reducing the error rate.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,278,675 to Kurbiyashi et al., which discloses waveform equalizer with an equalization characteristic as to emphasize high-frequency components.

b. J.P. Pub. No. 10-228733 to Nakatsu al., which discloses a phase shifter for shifting, responsive to a phase control signal, the phase of the read clock signal that has been output from the clock generator and outputting a phase-shifted read clock signal as a sampling clock signal, an A/D converter for converting the equalized signal into a digital read signal by sampling equalized signal by reference to the sampling clock signal that has been output from the phase shifter; and a phase control signal generator for detecting a phase deviation of the sampling clock signal in accordance with the digital read signal that has been output from the A/D converter and outputting the phase control signal to the phase shifter so as to reduce the phase deviation of the sampling clock signal, wherein a decoder generates the digitized data from the digital read signal that has been output from the A/D converter

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jorge L Ortiz-Criado whose telephone number is (703) 305-8323. The examiner can normally be reached on Mon.-Thu.(8:30 am - 6:00 pm),Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H To can be reached on (703) 305-4827. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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